ABSTRACT

The objective is to provide a data transfer control device and electronic equipment that are capable of reducing processing overheads, thus enabling high-speed data transfer within a compact hardware configuration. During IEEE 1394 data transfer, a packet assembly circuit (280) reads a header and data for a packet from header and data areas in a RAM (80) and links them together. The period of time during which a header CRC is created is used to obtain a data pointer. Whether a header or data is being read is determined by tcode, and the header pointer or data pointer incremented accordingly. A header is created while data is being fetched from the data area. Data is fetched to one channel which a packet is being transmitted from another channel within a divided send packet area. A linkage pointer is used to sequentially read a packet from another channel. An ACK code from the transfer destination is written back to the channel that sent the corresponding packet. Packets can be sent in series by rewriting a basic header to sequentially create headers until a number-of-repeats reaches zero.